MicroBooNE DAQ Status

Eric Church, Yale

LANL LArTPC Meeting

1-Feb-2013

Outline

- Overview
- MicroBooNE DAQ Teststands
  - People/Institutions
- MicroBooNE DAQ System Overview
- System Components at DAB Teststand
- Progress so far
- Electronics Status
- Ongoing Work: stuff we're still building
- Charge Injection Calibration
- Schedule to completion
- Summary and Outlook
- Considerations for LANL LArTPC

MicroBooNE Status

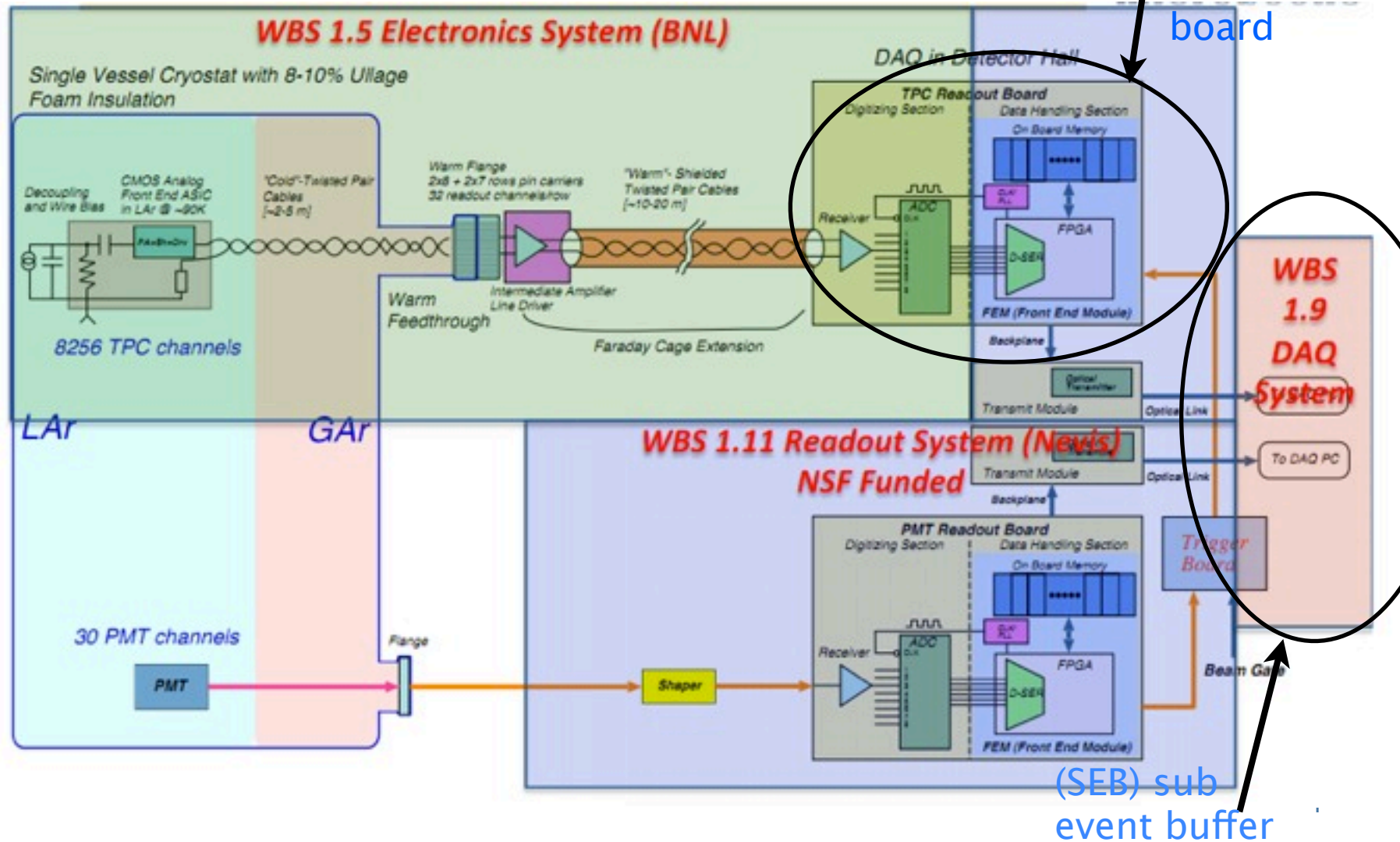- See Wes's talk
- CD3b March, 2012.
- CD4 in Summer, 2014
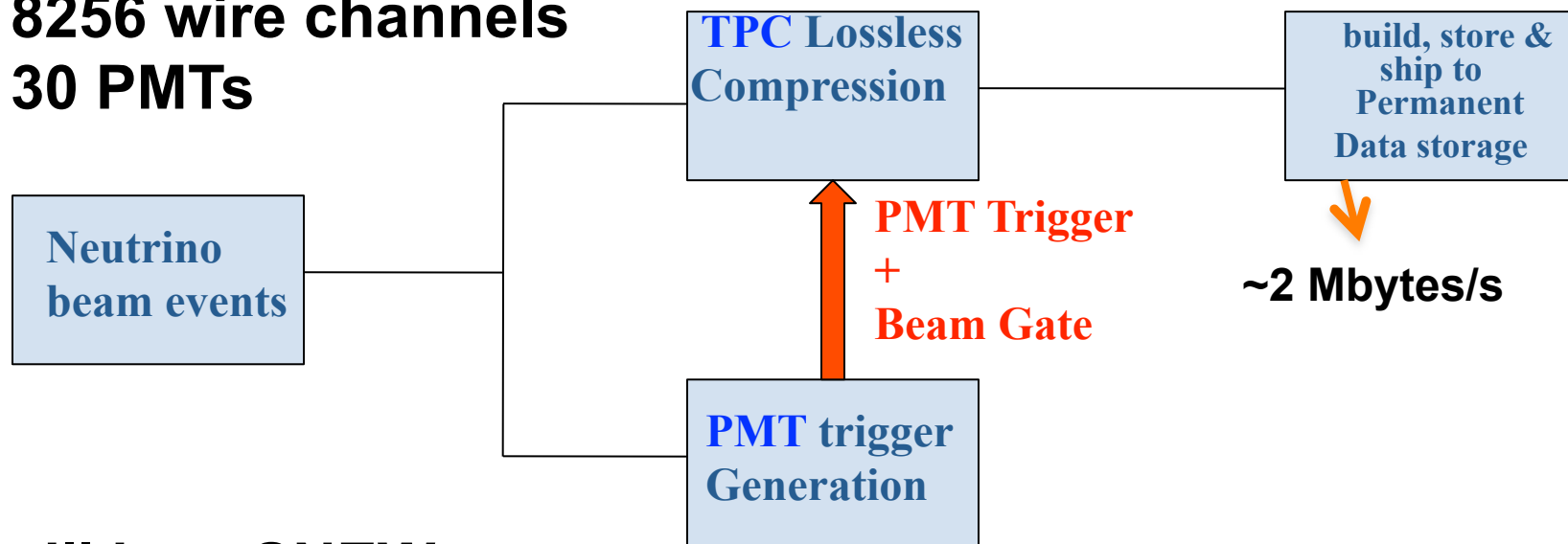 - MicroBooNE collaboration and project hope to be ready much earlier.

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System Overview

□ **standard words/pictures**

(FEB or FEM) front end board

(SEB) sub event buffer

Digitizing Boards: MicroBooNE design

8256 wire channels
30 PMTs

Neutrino beam events

TPC Lossless Compression

build, store & ship to Permanent Data storage

PMT Trigger + Beam Gate

~2 Mbytes/s

PMT trigger Generation

We will be a SNEWs _consumer_.

Continuous TPC and PMT readout

Supernova events

TPC and PMT Compression, decimation

local server Cyclic(2day) Data storage

50-100 Mbytes/s/crate (7 TB/day)s
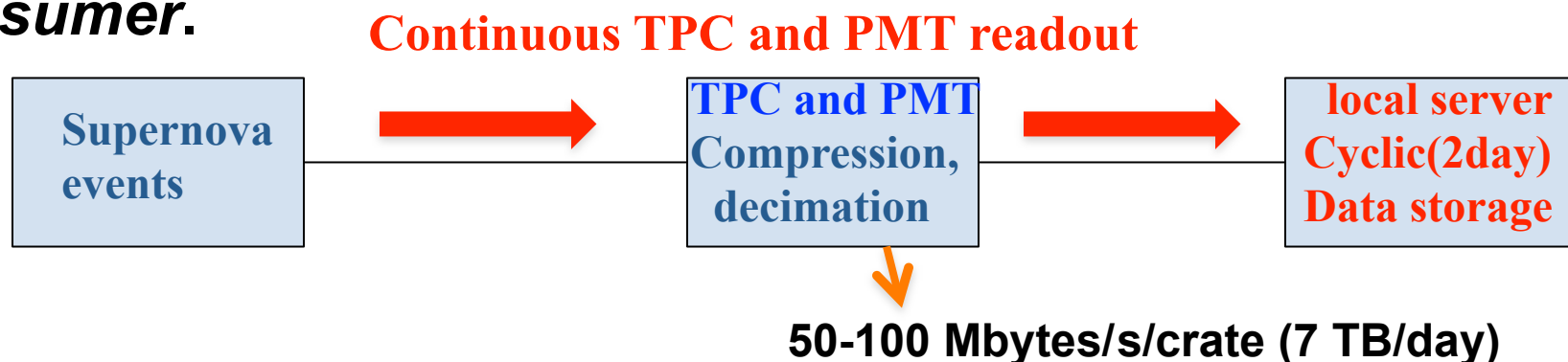
Use the SN data stream to select and study K background events

Resources

- Work on the DAQ is ongoing at Nevis/FNAL through 2013. Moving to LArTF (MicroBooNE enclosure), we hope, end of 2013.

- The DAQ team is comprised of the following people :
  - Yale: Eric Church (TD), Andrzej Szelc (postdoc)
  - LANL: Wesley Ketchum and Zarko Pavlovic
  - Nevis: Georgia Karagiorgi, David Kaleko
  - Va Tech: Camillo Mariana and Leonidas Kalousis
  - KSU: Glenn Horton-Smith, David McKee and Sowjanya Gollapinni
  - FNAL:Bruce Baller (L2), Ron Rechenmacher, Gennadiy Lukhanin, Kurt Biery (FNAL CD CET group engineers)
  - MIT: Matt Toups, Ben Jones, Christie Chiu
  - UT-Austin: Rashid Mehdiyev

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D0 (DAB) and Nevis Teststands

- This talk will mostly focus on the DAB (D0 Assembly Building) teststand, on which the MicroBooNE DAQ team is developing the DAQ.

- Nevis runs its own test stand, where they run code and pass knowledge to us. And also, where they perform characterization of the electronics as it is fabricated and shipped to them.
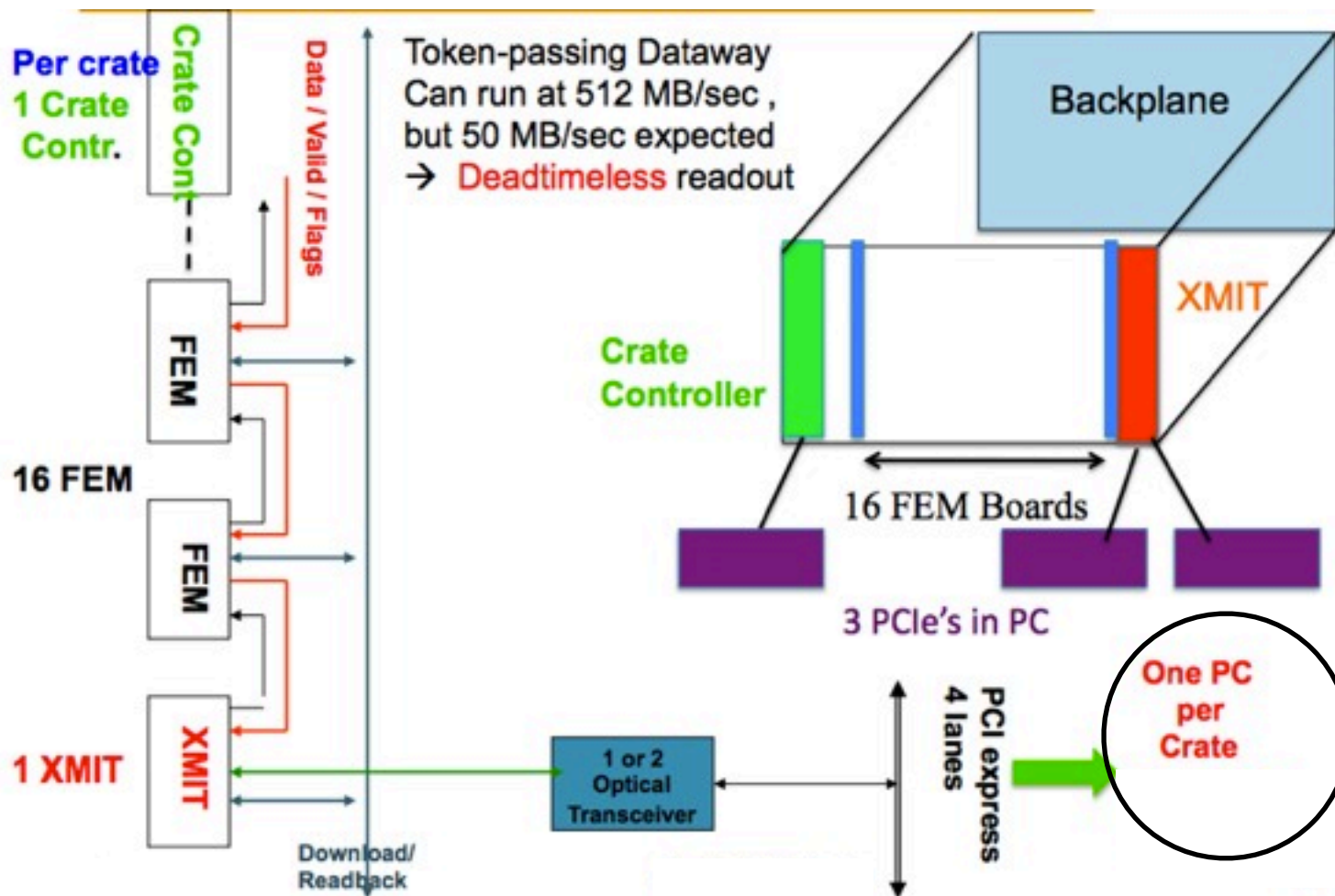
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Other uB-related Test Stands

☐ BNL maintains a front-end electronics test stand at which they test ASICS, motherboards, pre-amps, intermediate amplifiers, ...

☐ There is a Test Stand at PAB at FNAL that uses the control card (not XMIT) to read data from PMTs in liquid argon.

- No wires, no E-field, reading out through Controller Card.
- They are reading PMTs, and fitting to early/late light components
- Doing dE/dx studies with an alpha source
- Nitrogen impurity measurement
- Shaking out PMT DAQ components, generally

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Nevis TPC Crates (x9)

Per crate
1 Crate Contr.

Crate Cont.

Data / Valid / Flags

Token-passing Dataway
Can run at 512 MB/sec ,
but 50 MB/sec expected
→ Deadtimeless readout

Backplane

XMIT

Crate Controller

16 FEM

FEM

FEM

16 FEM Boards

3 PCIe's in PC

1 XMIT

XMIT

1 or 2 Optical Transceiver

PCI express 4 lanes

One PC per Crate

Download/ Readback

Wires are sampled@2MHz, 2 bytes

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Fibers into SEB-computers

SEB == Sub Event Buffer <==> basically one crate.

Often SEB refers to the computer servicing that crate.

There are two data streams.
(1) Triggered
(2) Supernova:
    continuous stream

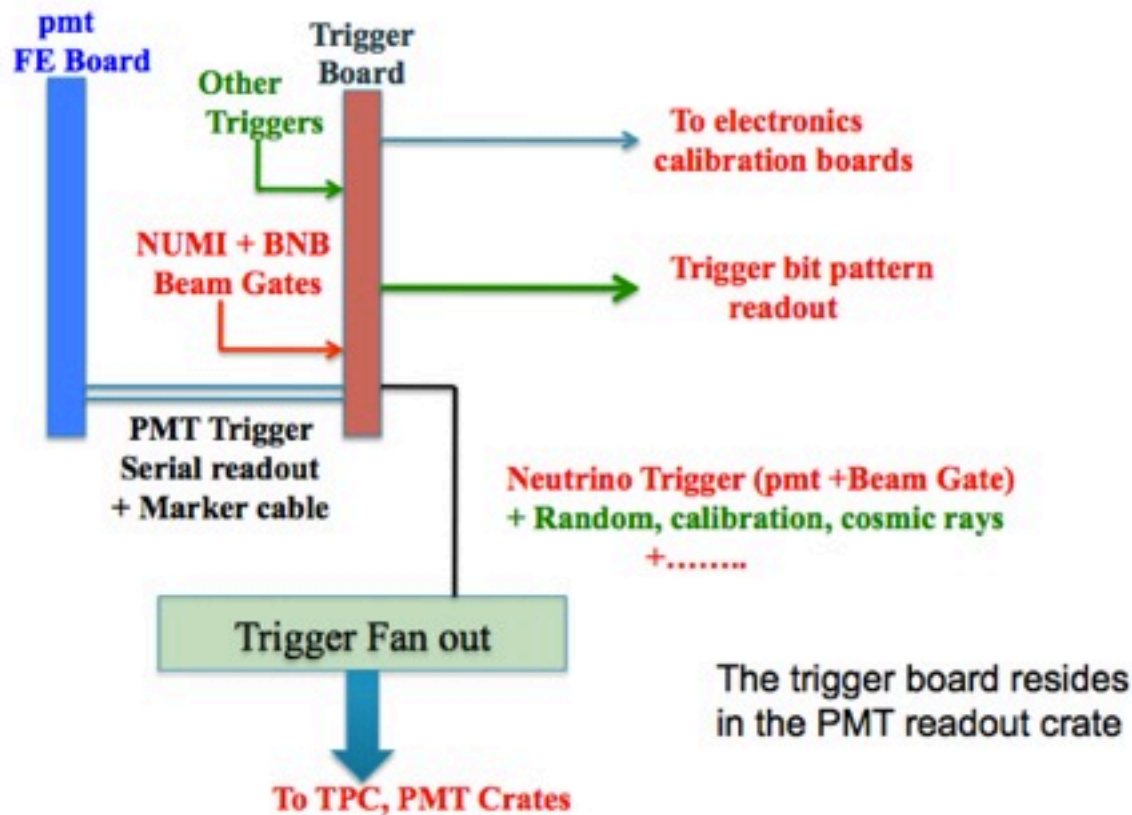Both come through the "XMIT" card on duplex fibres.
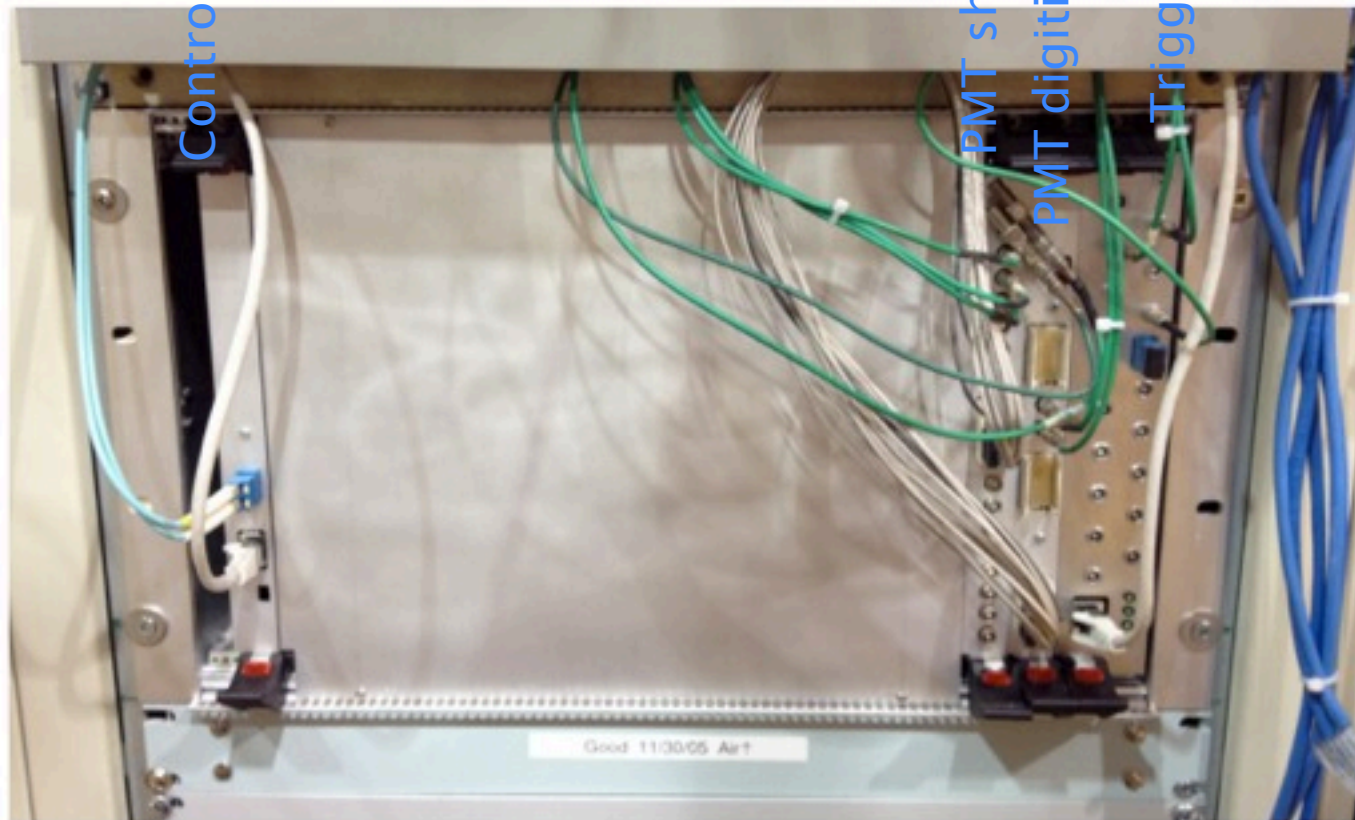
Three NEVIS custom PCIe cards per SEB.

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Nevis Trigger Crate

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PAB Teststand

Controller card

PMT shaper card

PMT digitizer FEM card

Trigger board

Good 11/30/05 Air1

PMTs sampled@64MHz, 2bytes

Figure 2: PMT Crate Physical Setup (as of Oct. 10, 2012)
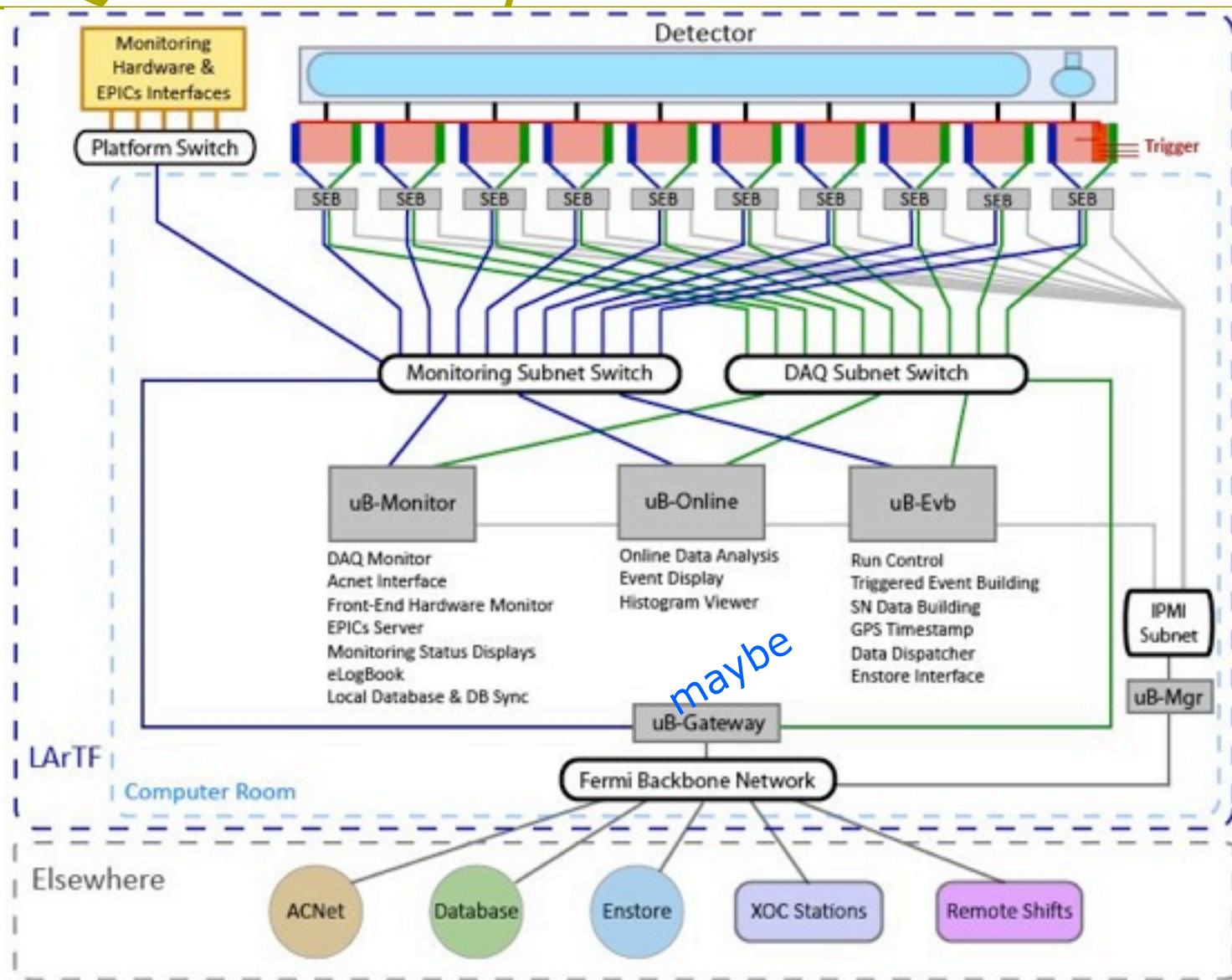
1–Feb–

Overview of DAQ Project: WBS 1.9

- The MicroBooNE DAQ picks up where 1.11 (Nevis electronics) hands the data off: through the PCIe cards in the SEBPCs.

- DAQ is responsible for reading out, assembling events, writing them to file.

- But also:
  - Monitoring and Control,
  - Beam data concatenation,
  - Run stop/start: State Machine
  - Calibration runs, Laser Runs, …
  - Online and Nearline processes,
  - File management, …

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DAQ Network/Process Overview

□ # BNL: ASICs through ADC

NIM pulsing logic

Intermediate amplifiers

ASICs config over USB

uboonedaq-seb-01.fnal.gov

BNL ADCs + NEVIS FEMs

Crate Power

wire bias and ASICs power

motherboards

"toy TPC"
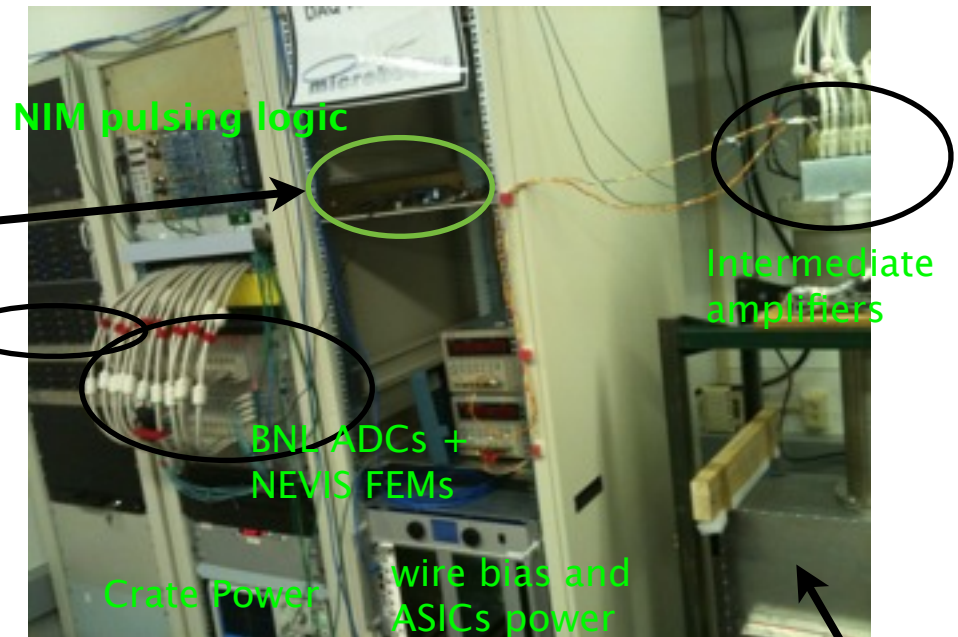
□ # Nevis readout:

- ▪ Crate cards through PCIec ards

□ # DAQ: computers, software, glue

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Technical Progress since CD-2

- Glomation SBC as the slow mon/control hub: one per rack.

- ACNET data, file management will come from supported CD IF Data Logging project and CD Enstore/Sam solutions, respectively: Zarko!

- Readout established

- State Machine Built

- Code build specified
  - We have a very extensible model: ups'es where possible, git repository, CMake build system, C++ codebase

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Glomation Single Board Computer GESBC–9G20

- SBC includes
  - Linux OS
  - Ethernet
  - RS232
  - USB
  - 40 digital I/O
  - 4 ADC
  - I2C and SPI bus

Glomation
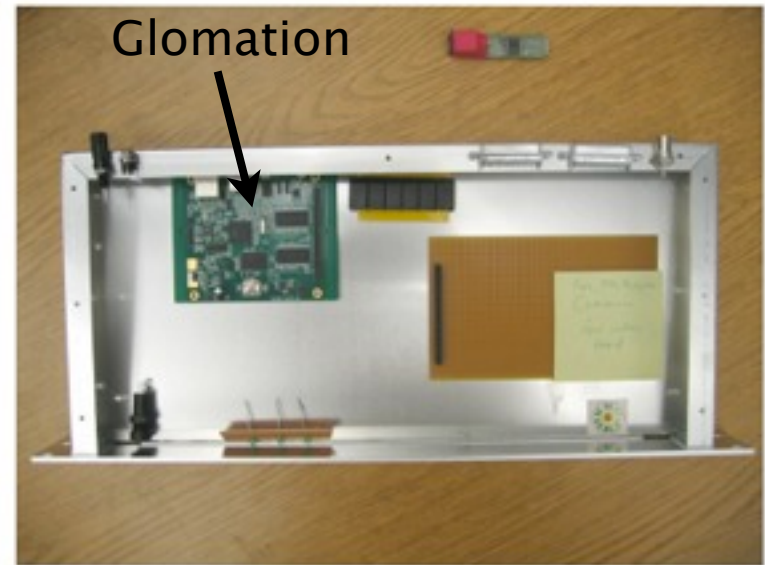
- Interfaces directly with
  - **Glassman Drift HV – RS232**
  - **Rack Temperature – I2C bus using Maxim DS1624**
  - **Rack Fanpack – digital I/O**

Glenn Horton–Smith, KSU

Technical Progress, contd

❑ EPICs IOCs (Input/Output controllers) accessing shared memory already demonstrated. SMNP to control/monitor most power supplies and monitor computer environment variables.

❑ Online data health via Ganglia: very powerful http-served monitoring tool. – Gennadiy L.

  o JSON plots, ala finance.google.com, etc

  o Easily scaled and intuitive

  o Simply, define the metric in the code. Time-series chart appears, nicely laid out. Layout is easily configurable.
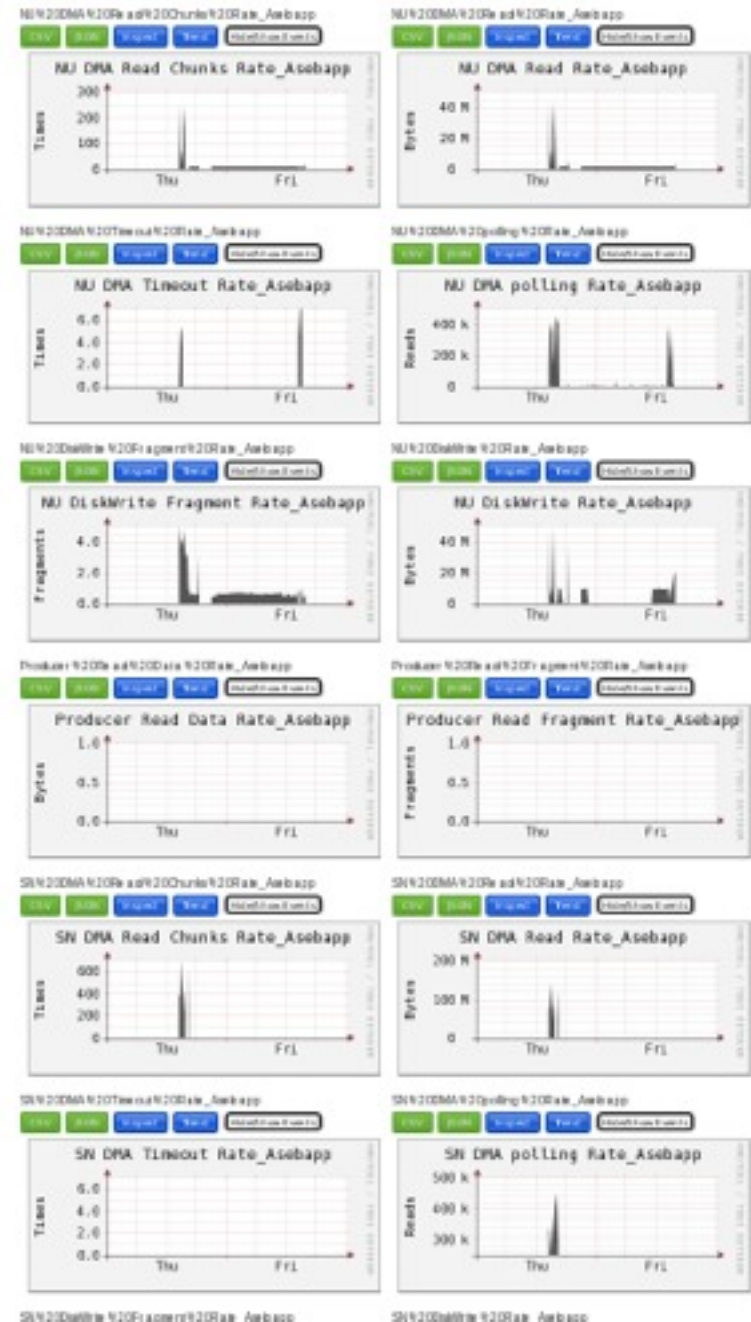
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Ganglia

Custom Metrics

For Online Monitoring of raw
system, and also stuffed at the
~1Hz level into EPICS slowmon dB

Trig
DMA
Rate

Assem
–bler
write
Rate

SN
DMA
Rate

Status of Work: recent accomplishments

- Event building finished (experience from mBooNE). Have even done it with uBooNE-specific DMA'd data files. A full, detailed fake data transport mode completed. -- Wes

  - it remains to exercise this on multiple actual crates, live -- Fall, 2013.

- Serialized/archived output data format defined. In a boost::serialized class

  - "serialized", "archived" meaning data laid out in order, with versioning that makes everything backward compatible as code evolves

  - Methods to write out binary chunks into file and read it back and unwind it to level desired -- Again, Wes.

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Electronics Status

- Next few slides

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BNL fabrication and testing

These are so-called Cycle 4* ASICs. Final Cycle.

- CMOS Analog Front End ASIC
  - ASICs were delivered in early December
  - ASIC incoming test is ongoing at room temperature
    - 593 ASICs have been tested, 529 ASICs passed the test
    - Yield is ~89.2%
  - ASIC cold screening test is finished
    - 201 ASICs have been tested in LN_2, 195 ASICs passed the test
    - Very stringent criteria to screen chips in LN_2, for 6 chips that did not pass the test
      - 4 chips: each has a channel with slightly a reduced dynamic range
      - 2 chips: each has a channel with a slightly larger undershoot
    - Cold/Warm Yield is ~97%

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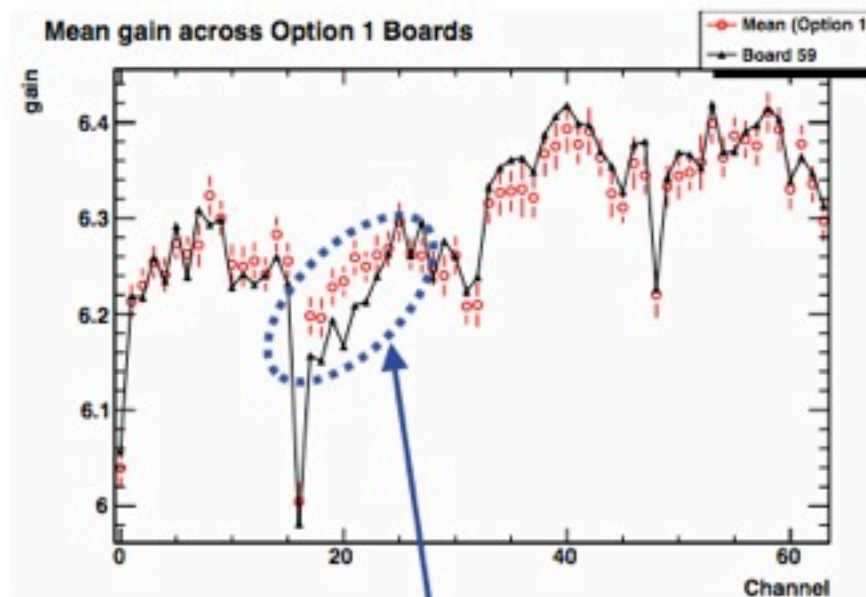
Electronics testing at BNL

ADC pedestals from reading signals with no input pulse.
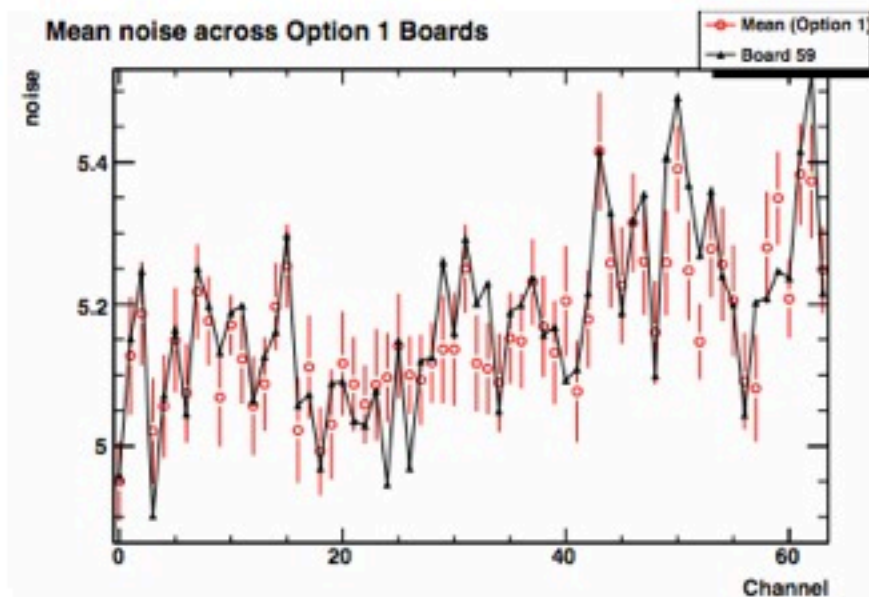
Calculated by pulsing multiple times at N~8 input amplitudes.

Noise looks OK.

Gain in some channels significantly low.

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BNL Nevis Electronics status

- Motherboard production fabrication starting next week. Received at BNL by end of March.
- ADC boards shipped/shipping now to NEVIS.

- Then, to DAB
- Into Racks in Spring

Nevis **Status**

- We now have >90% of boards in hand (from assembler):
  - All FEMs
  - All XMITs
  - All clock cards
  - All Controllers
  - All PMT shapers

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Status of Work: things in progress
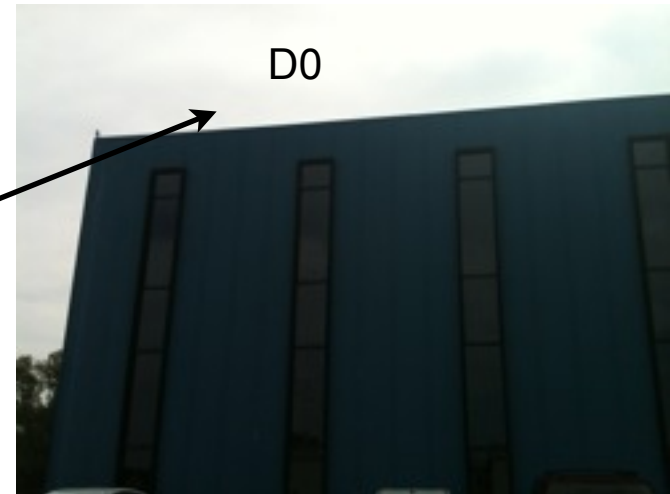
- Absolute time into header: GPS card
  - Code in place to allow Pulse Per Second (PPS) interrupt to capture/synchronize DAQ clock to GPS.

- Configuration Database

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GPS

In progress

D0

This $3k Symmetricom PCIe
card advertises
170 nsec accuracy.

VA Tech taking this on. Trigger card in next couple
months to store the DAQ clock value on each
GPS's Pulse Per Second input. We then will grab
that value and the GPS time and shove it into the
trigger data header. Will propagate to the overall
global header from there. All code already written.

PCIe card In uboonedaq-seb-10, works
with new antenna, driver, code.

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Configuration DB Scheme
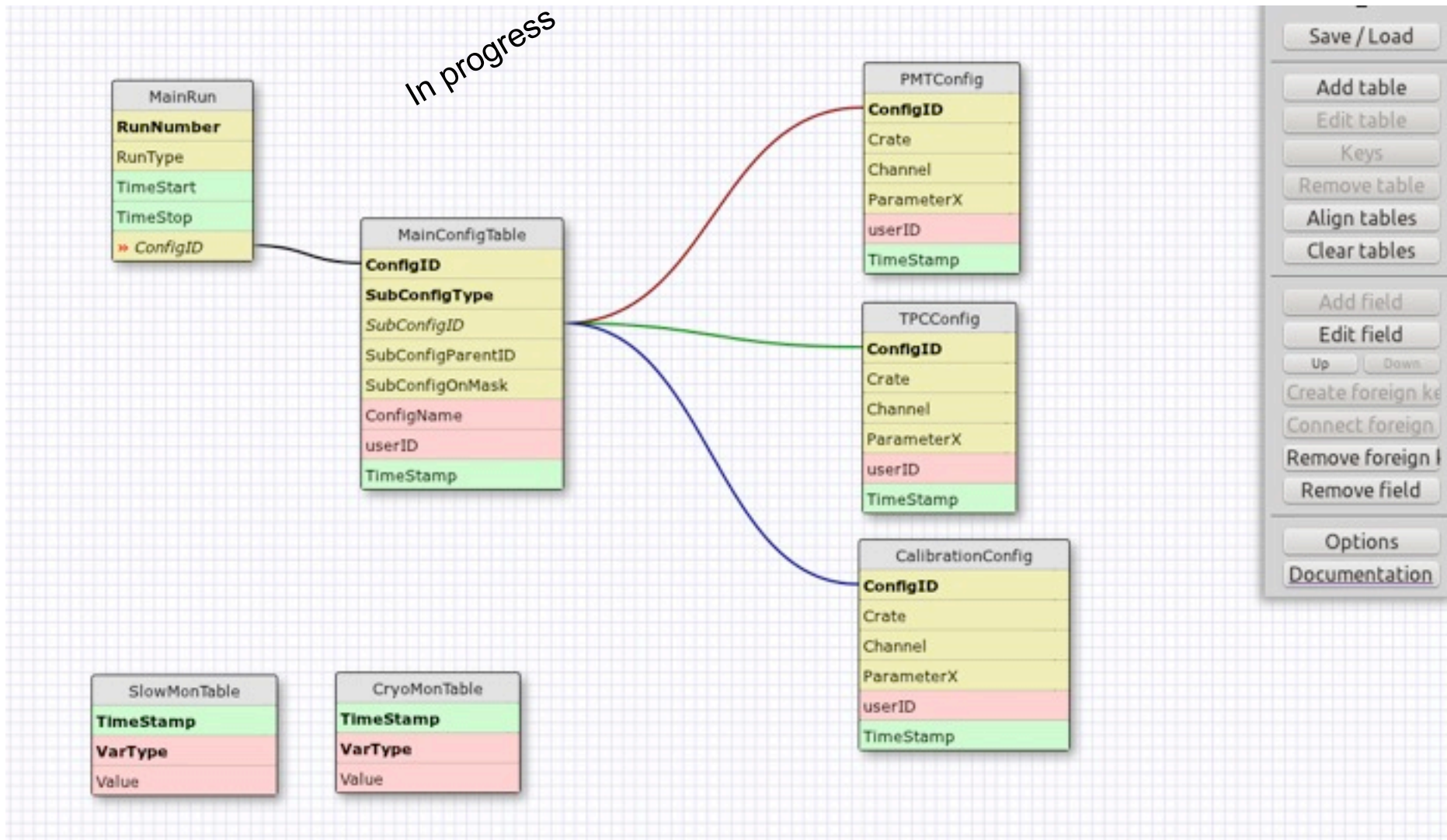
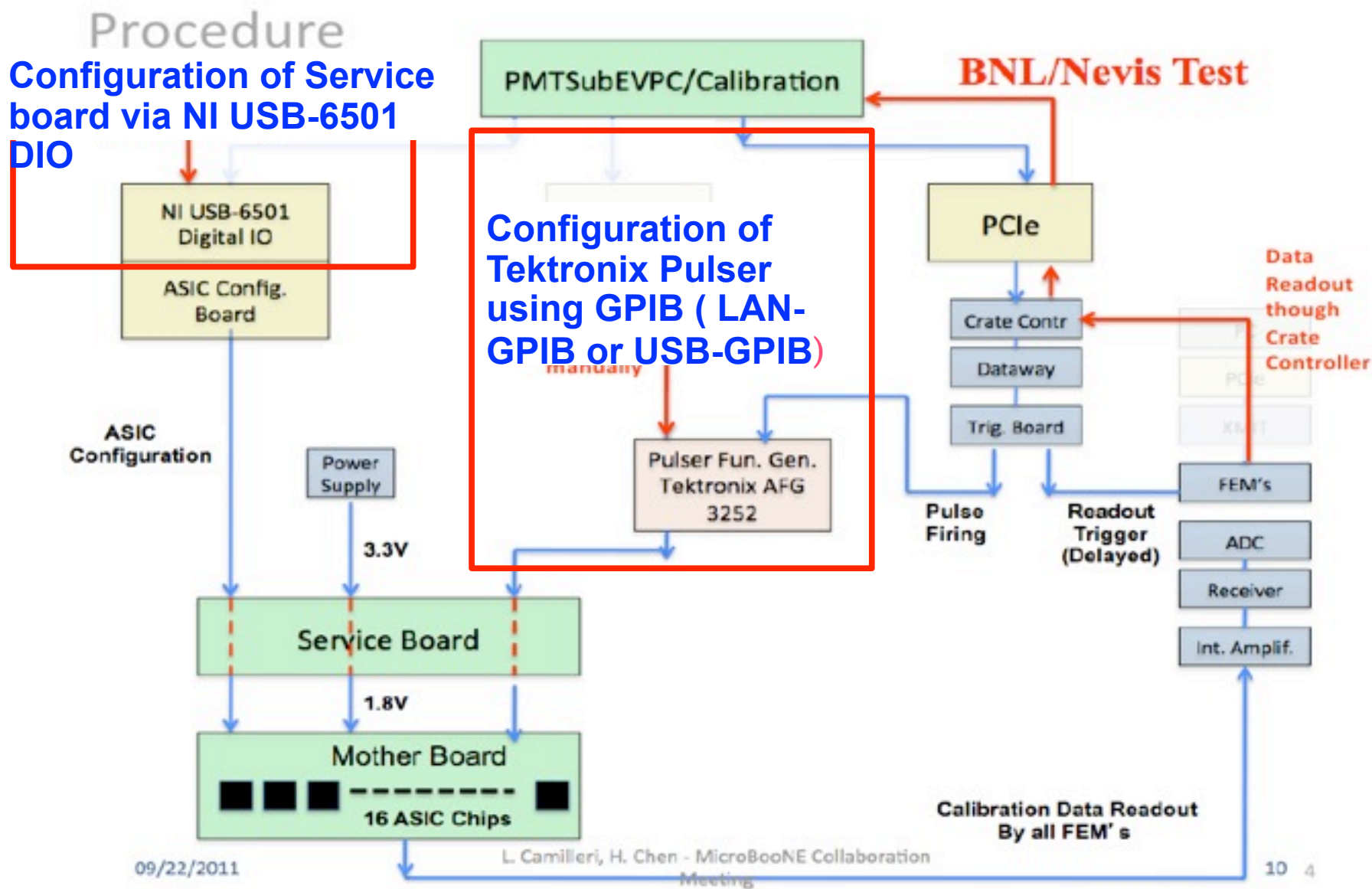Andrzej Szelc, Yale

Status of Work: things in progress 2

- Processes for Nearline monitoring (LArSoft)
  - Swizzle from RawData
- EPICS, ongoing
  - Server imminently to be installed on its machine,
  - Alarming, Archiving, Control/Display GUI
  - IOCs reporting all data on list to EPICS dB
- Understanding nuances of Readout and FEM FPGA code ...
  - Interfacing with NEVIS

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Status of Work: things in Progress 3

☐ Message Passing System to effect State Machine transitions: Configure, Connect, Run, Pause, Configure, Run, Stop, etc.

- Code does not just fall through. This is a crucial step of sophistication that allows multi-mode running
- Done to 0th order.
- But now development for Calibration runs is needed: we want to run the special calibration trigger and configure hardware and pulse/read Nx1000 times all within one unambiguously labeled run with subruns: Pause, Re-config hardware, pulse/read, Pause, etc.

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Calibration Hardware

Procedure

Configuration of Service board via NI USB-6501 DIO

Configuration of Tektronix Pulser using GPIB (LAN-GPIB or USB-GPIB)

BNL/Nevis Test

PMTSubEVPC/Calibration

PCIe

NI USB-6501 Digital IO

ASIC Config. Board

Crate Contr

Dataway

Trig. Board

Data Readout though Crate Controller

ASIC Configuration

Power Supply

Pulser Fun. Gen. Tektronix AFG 3252

3.3V

Pulse Firing

Readout Trigger (Delayed)

FEM's

ADC

Receiver

Int. Amplif.

Service Board

1.8V

Mother Board

■ ■ ■ – – – – – – – – ■
16 ASIC Chips

manually

Calibration Data Readout By all FEM's
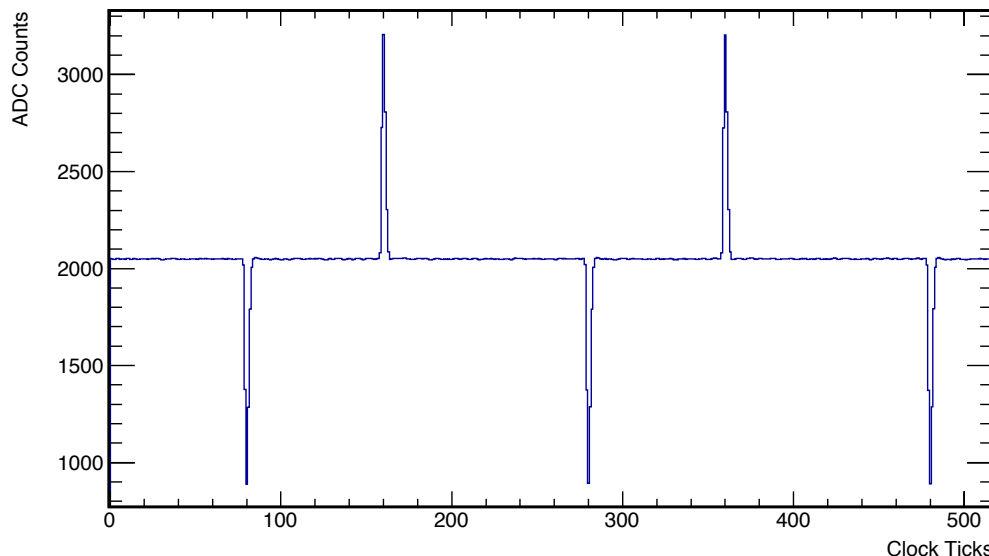
09/22/2011

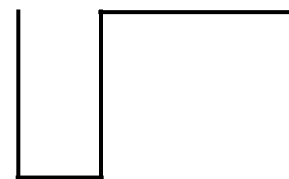L. Camilleri, H. Chen - MicroBooNE Collaboration Meeting

10   4

Calibration Run: we've done it

Continuous Pulse. Needs to be Burst
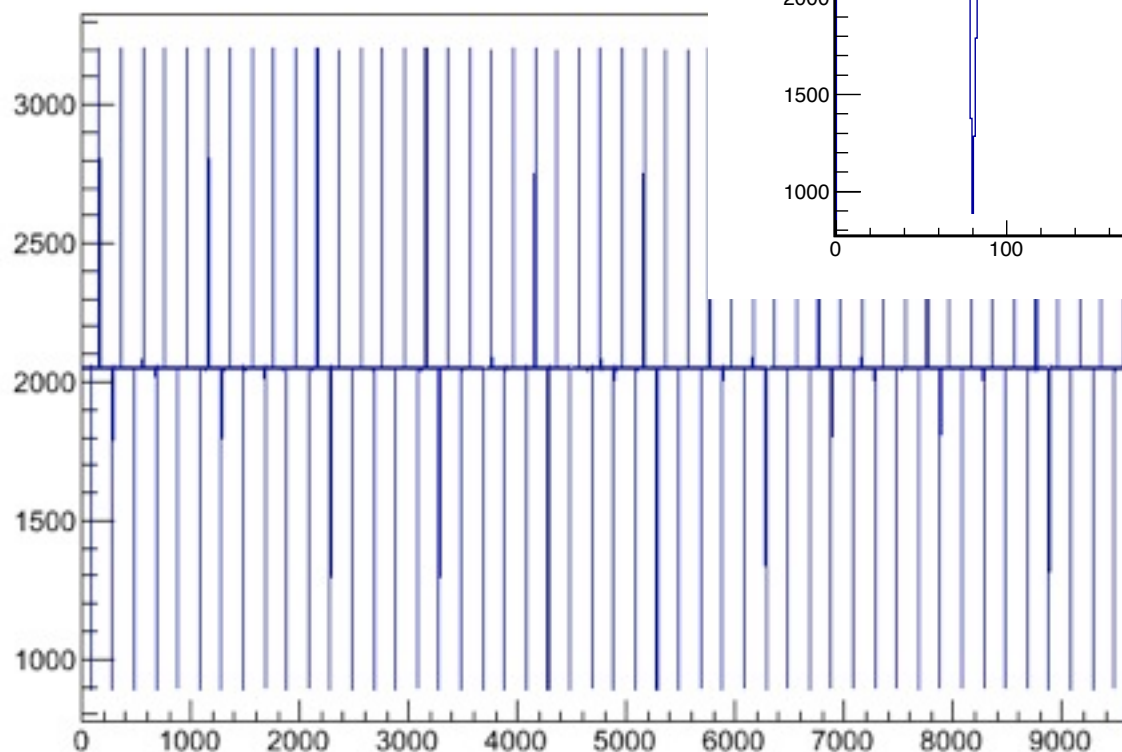
The input signal is 10 kHz.
It is a negative-, then positive-going square-wave signal, of width 40 usec.

Full 3x1.6msec frame read-out.

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Schedule Highlights

CY 2012   CY 2013   CY 2014

| Q1 | Q2 | Q3 | Q4 | Q1 | Q2 | Q3 | Q4 | Q1 |
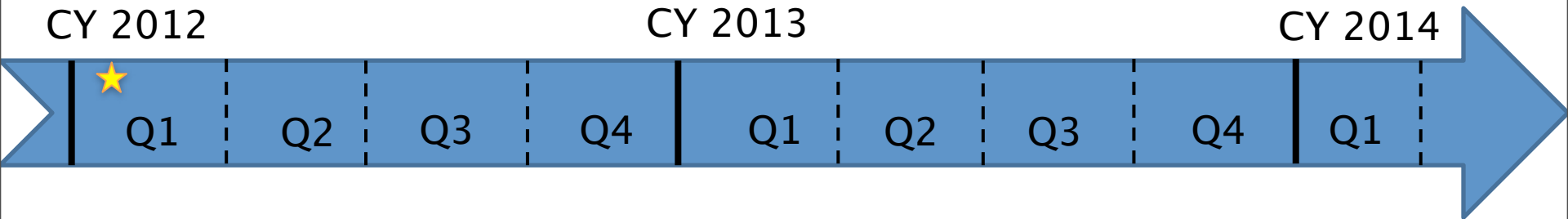
⭐ **Buy Pulser, get scope, PS's, test stand computers, start developing. CD3b!**

⭐ **D0 Test Stand: Readout Testing**

⭐ **Buy Glomations**

⭐ **Buy switches**

⭐ **Buy servers (L2 Milestone)**

⭐ **Electronics from BNL, Crates from Nevis arrive at D0, tested on TPC**
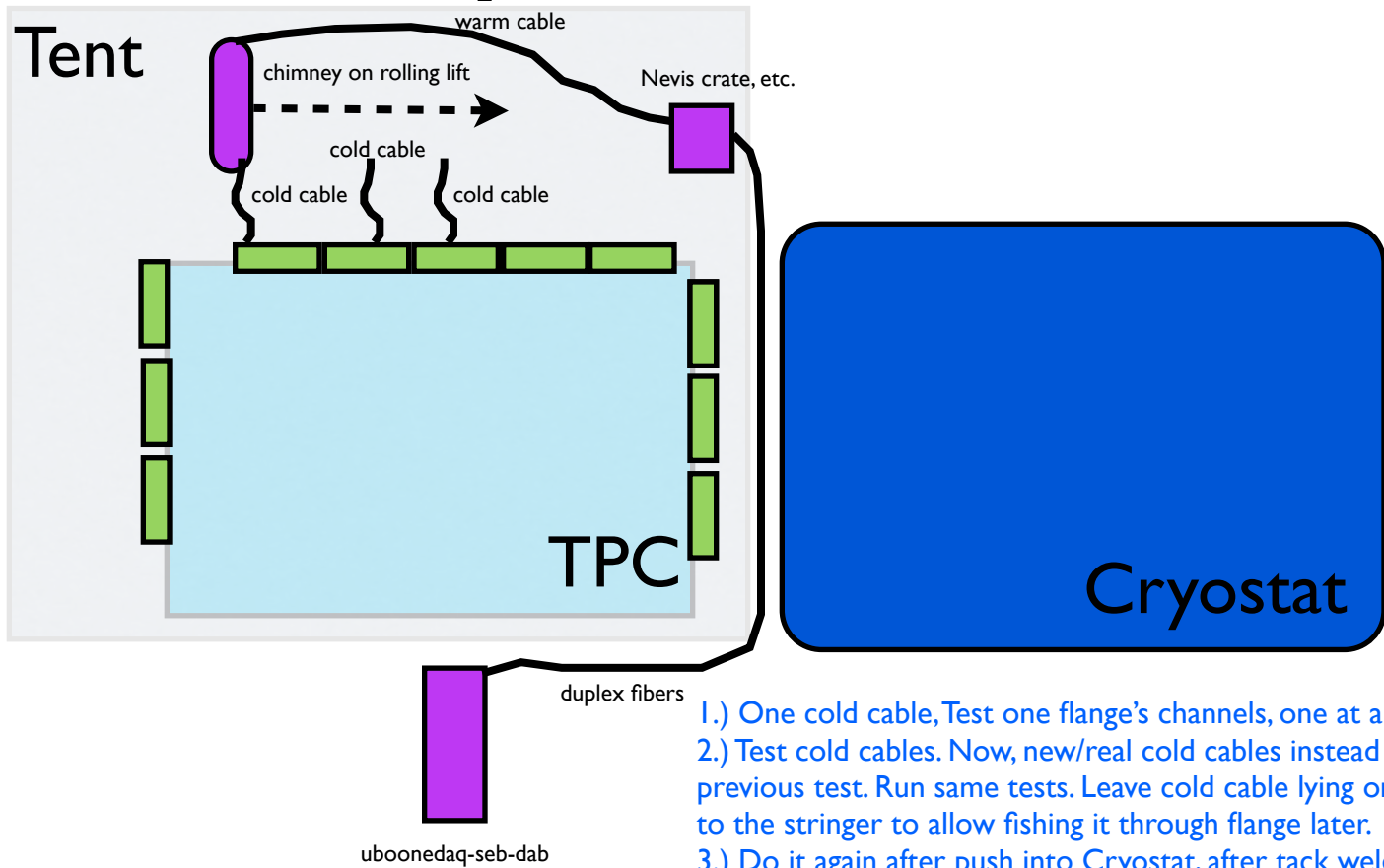
⭐ **Set Up DAQ server racks**

⭐ **System Ready**

Test Stands through 2013

- The Test Stand at DAB at FNAL will serve as an acceptance test station before buttoning-up, when/as all of the electronics boards are shipped to FNAL.

- 3-phase plan to test all Front End channels, keeping everything downstream fixed.

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FNAL DAB Tests: 3 phases

Tent

warm cable

chimney on rolling lift

Nevis crate, etc.

cold cable

cold cable   cold cable

TPC

Cryostat

duplex fibers

uboonedaq-seb-dab

1.) One cold cable, Test one flange's channels, one at a time.
2.) Test cold cables. Now, new/real cold cables instead of the one from previous test. Run same tests. Leave cold cable lying on top of TPC tied to the stringer to allow fishing it through flange later.
3.) Do it again after push into Cryostat, after tack weld, after real weld, after move to LArTF

MicroBooNE DAQ Summary and Outlook

- ❑ D0 Assembly Building test stand work is in full production, and ramping up further. Eye on everything becoming eventually the full DAQ.

- ❑ Move to FEE installation this Spring. Electronics Acceptance testing prior to buttoning up in Fall, move by Q1, 2014, perhaps earlier, with LAr Fill following (off project).

- ❑ Procurement of DAQ hardware ongoing: computers, switches, fibers, pulsers … Major p.o.'s going out the door imminently.

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LANL LArTPC considerations

- 900? channels: 64*16 channels in one Nevis crate.

- N TPC crates. Sounds like N=1

- Need to hold 3N PCIe cards, 4 in PMT/trigger crate

- 2U Koi SuperMicro boxes can hold 3 PCIe full height cards with a riser card and a RAID controller card.
  - 10 GbE network cards take another slot
  - GPS card may take another
  - 4U box can hold 6 slots with riser

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LANL LArTPC: Using the Codebase

□ In principle, you just pull it down

- `kinit -l user@FNAL.GOV`
- `git clone ssh://p-uboonedaq@cdcvs.fnal.gov/cvs/projects/uboonedaq/`
- `make -j32 # fast, parallel build on 32 cores`

□ Certainly, it won't build right out of the box

- We have some machine/environment specific things that will need reconfiguring
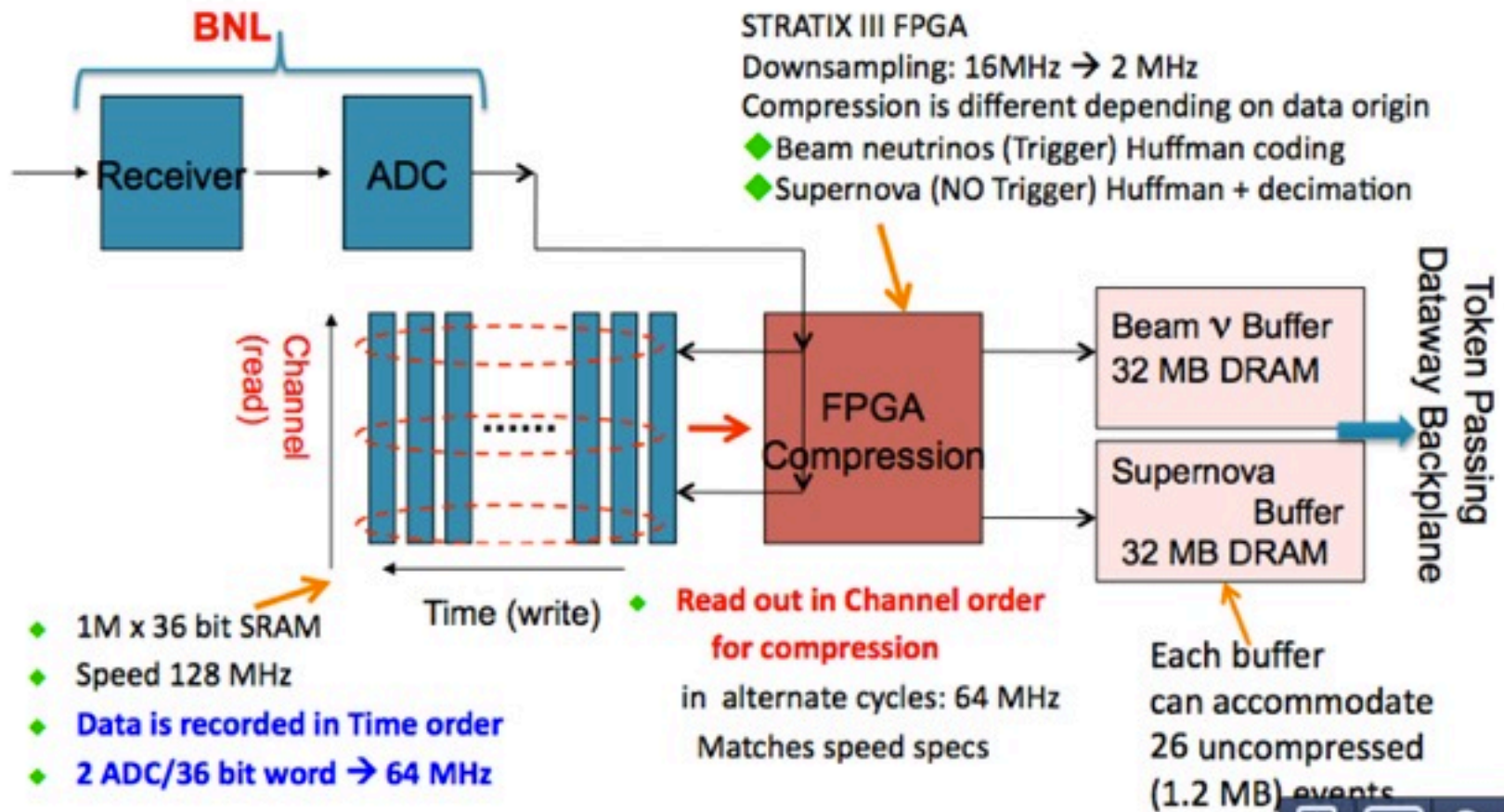
□ But, one could be on one's way

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Backup Slides

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Overview: Digitizing Boards: Hardware and Tasks

Continuous Data rate per card: 64 wires x 2 MHz = **128 MHz** 12 bit ADC words.

BNL

Receiver → ADC →

STRATIX III FPGA
Downsampling: 16MHz → 2 MHz
Compression is different depending on data origin
◆ Beam neutrinos (Trigger) Huffman coding
◆ Supernova (NO Trigger) Huffman + decimation

Channel (read)

Time (write)

FPGA Compression

Beam ν Buffer 32 MB DRAM

Supernova Buffer 32 MB DRAM

Token Passing Dataway Backplane

- 1M x 36 bit SRAM
- Speed 128 MHz
- **Data is recorded in Time order**
- **2 ADC/36 bit word → 64 MHz**

- **Read out in Channel order for compression**

  in alternate cycles: 64 MHz

  Matches speed specs

Each buffer can accommodate 26 uncompressed (1.2 MB) events

1·

Procurement * ~1.3

Package	Preparer	Estimated Cost	Requisition	Purchase Order
Jungo WinDriver License	Eric Church	6500	15-March-2012	
Glomation 9G20	Eric Church	125	30-March-2012	
Tektronix AFG3000 pulser	Eric Church	3400	30-March-2012	
GPS PCI card	Eric Church	3500	30-March-2012	
DS1624 digital thermometers	Eric Church	800	30-March-2012	
PMT SEB computer	Eric Church	5400	30-March-2012	
Three network switches	Eric Church	15000	1-March-2013	
Ten SEB computers	Eric Church	59000	1-March-2013	
Event Builder Computer	Eric Church	8500	1-March-2013	
Two Online Monitoring computers	Eric Church	10800	1-March-2013	
Slow mon/control EPICs computers	Eric Church	5400	1-March-2013	
On-platform computer	Eric Church	3200	1-March-2013	
Three slide-out monitor/keyboards	Eric Church	1000	1-March-2013	
14 Glomation 9G20 SBCs	Eric Church	800	1-March-2013	
Two shift station computers and monitors	Eric Church	14000	1-March-2013	